

PTMQ45

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	-INTR_A	-INTR_B	-INTR_C	-INTR_D	IDSEL	REQ/GNT
PCI 1	-INTR_F	-INTR_G	-INTR_H	-INTR_E	AD 16	0
PCI 2	-INTR_G	-INTR_F	-INTR_E	-INTR_H	AD 17	1

CLR_CMOS	
1 - 2	* Normal Operation
2 - 3	Clear CMOS



Front Audio	
Enable	Open
Disable *	Short (default)



KB_PWR : PS_KB & MS	
1 - 2	* 5VDDUAL
2 - 3	VCC



MFG_MODE	
OPEN	ME enable
CLOSE	ME disable



PLED_S: LED FUNCTION	
1 - 2	* DUAL LED
2 - 3	SINGLE LED



TPM_EN	
OPEN	TPM disable
CLOSE	TPM enable



Polyswitch Name	Current	Voltage	Page
KBFS	*	*	*
MSFS	*	*	*
KMFS	1.1A~1.5A	6V~8V	26
S5KBFS	*	*	*
USBFS1	*	*	*
USBFS2	*	*	*
USBFS1/2	1.1A~1.5A	6V~8V	19
USBFS3	*	*	*
USBFS4	*	*	*
USBFS3/4	1.1A~1.5A	6V~8V	19
USBFS5	*	*	*
USBFS6	*	*	*
USBFS5/6	1.1A~1.5A	6V~8V	19
USBFS7	*	*	*
USBFS8	*	*	*
USBFS7/8	1.1A~1.5A	6V~8V	19
USBFS1-4	*	*	*
USBFS5-8	*	*	*
USBFS9/10	1.1A~1.5A	6V~8V	19
1394FS1	*	*	*
1394FS2	*	*	*
1394FS3	*	*	*
1394FS1/2	*	*	*
1394FS1-3	*	*	*
VGAFS	0.75A~1.5A	6V~8V	14
DVIFS	*	*	*
GAMEFS	*	*	*
BAT	*	*	*

LAN ID LABEL

SYSTEM LABEL

BAR_CODE

BAR_CODE

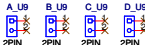
BIOS F.W AMI LABEL EN LR

ECN/BIOS 12*7mm LABEL

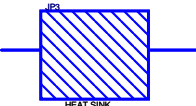
BAG



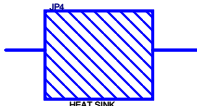
PE SHEET



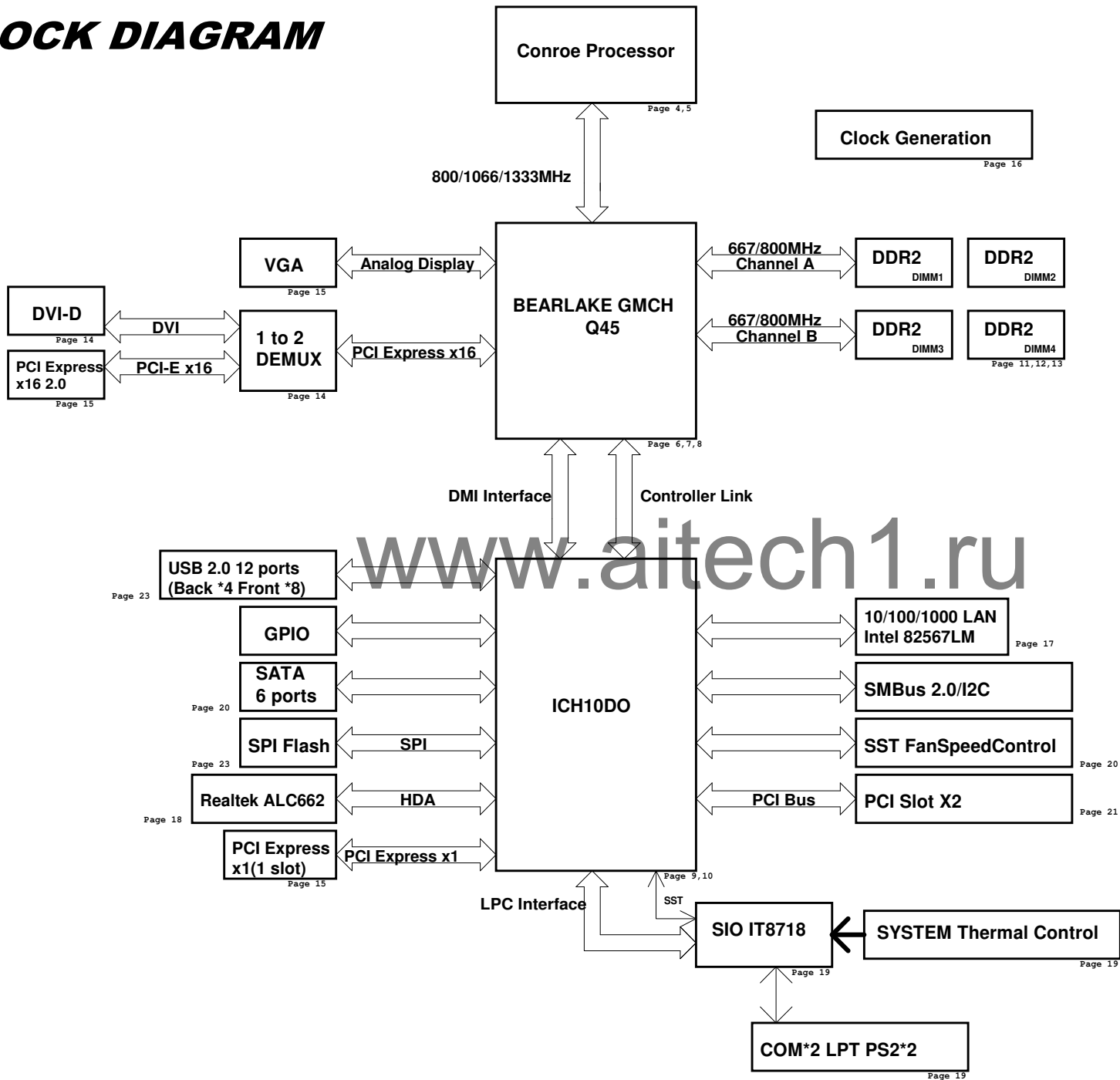
INTEL Q45 HEAT-SINK
24-20859-01



INTEL ICH10 HEAT-SINK
24-20441-01



BLOCK DIAGRAM

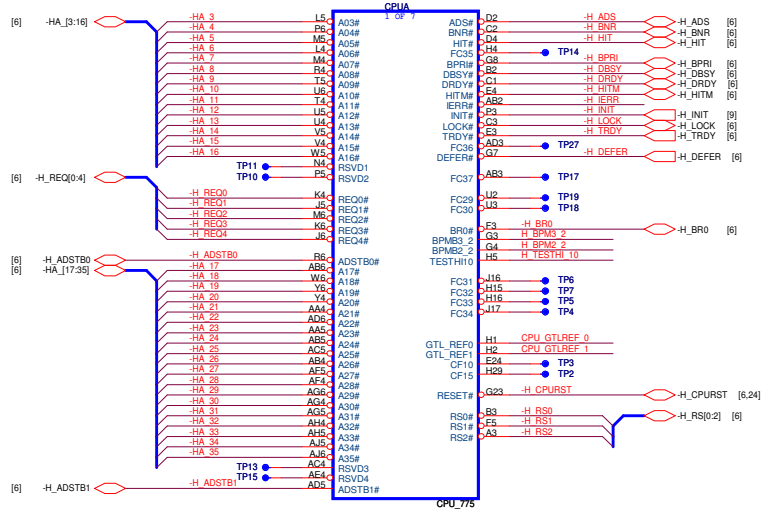


Project Name: PTQM45 V1.0.0 (04/15/2009)

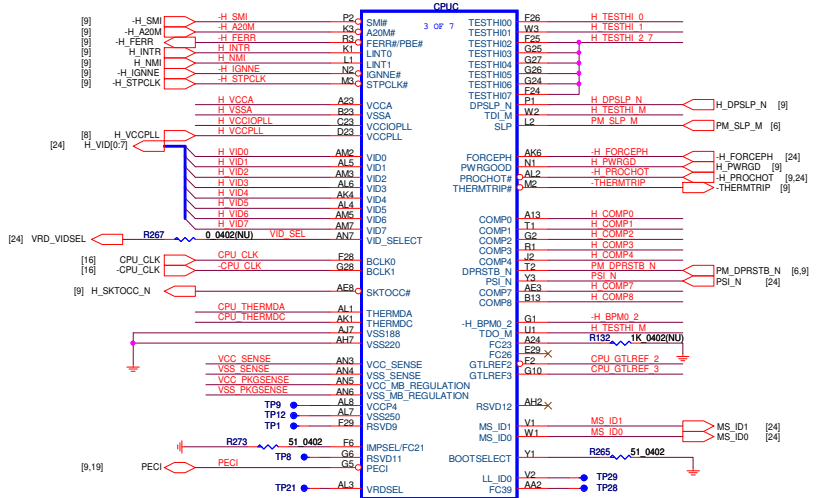
Change List..

Initial Version

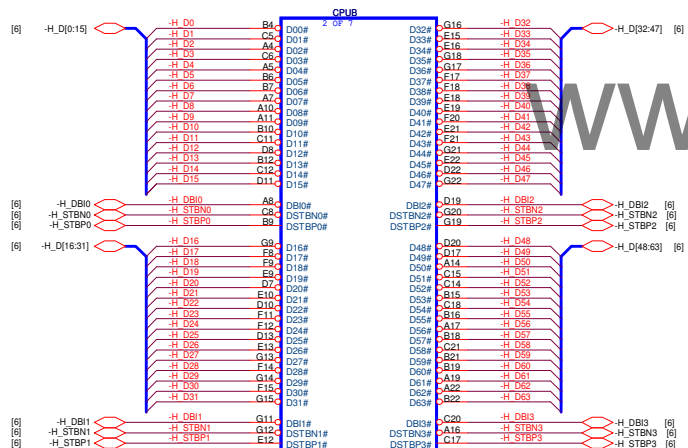
www.aitech1.ru

CPU LGA775-1

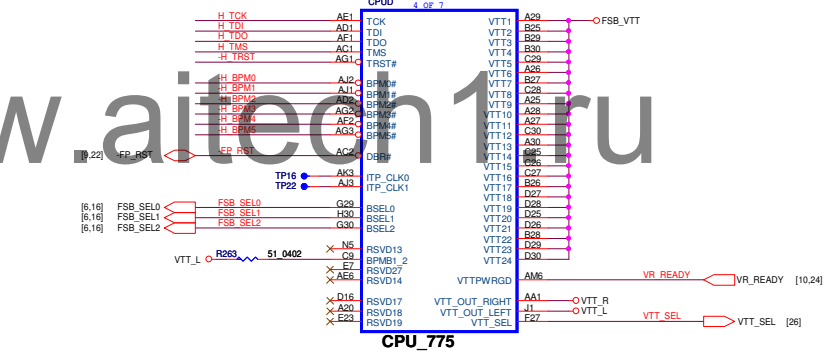
CPU_775P_Smithfield_V1.03



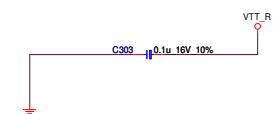
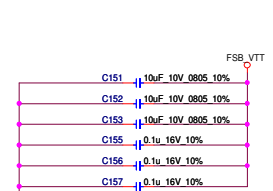
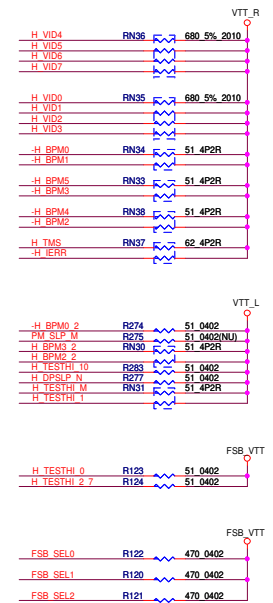
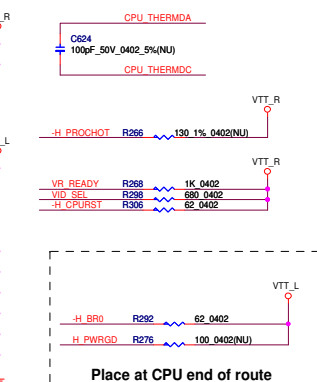
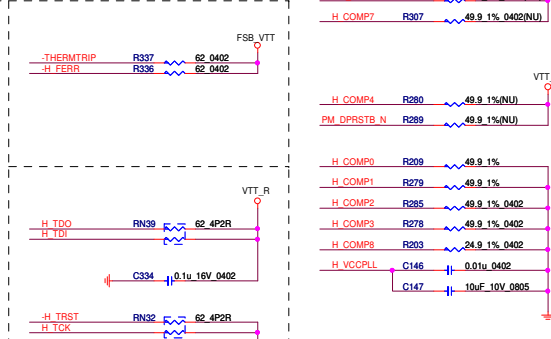
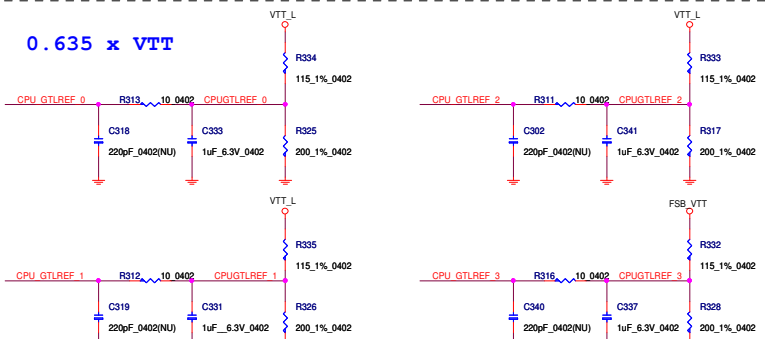
CPU_775



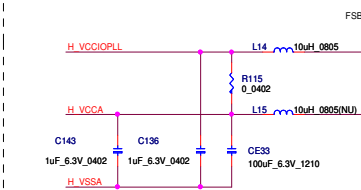
CPU_775



CPU_775



Place components as close as possible to processor socket trace width to caps must be no smaller than 12mil



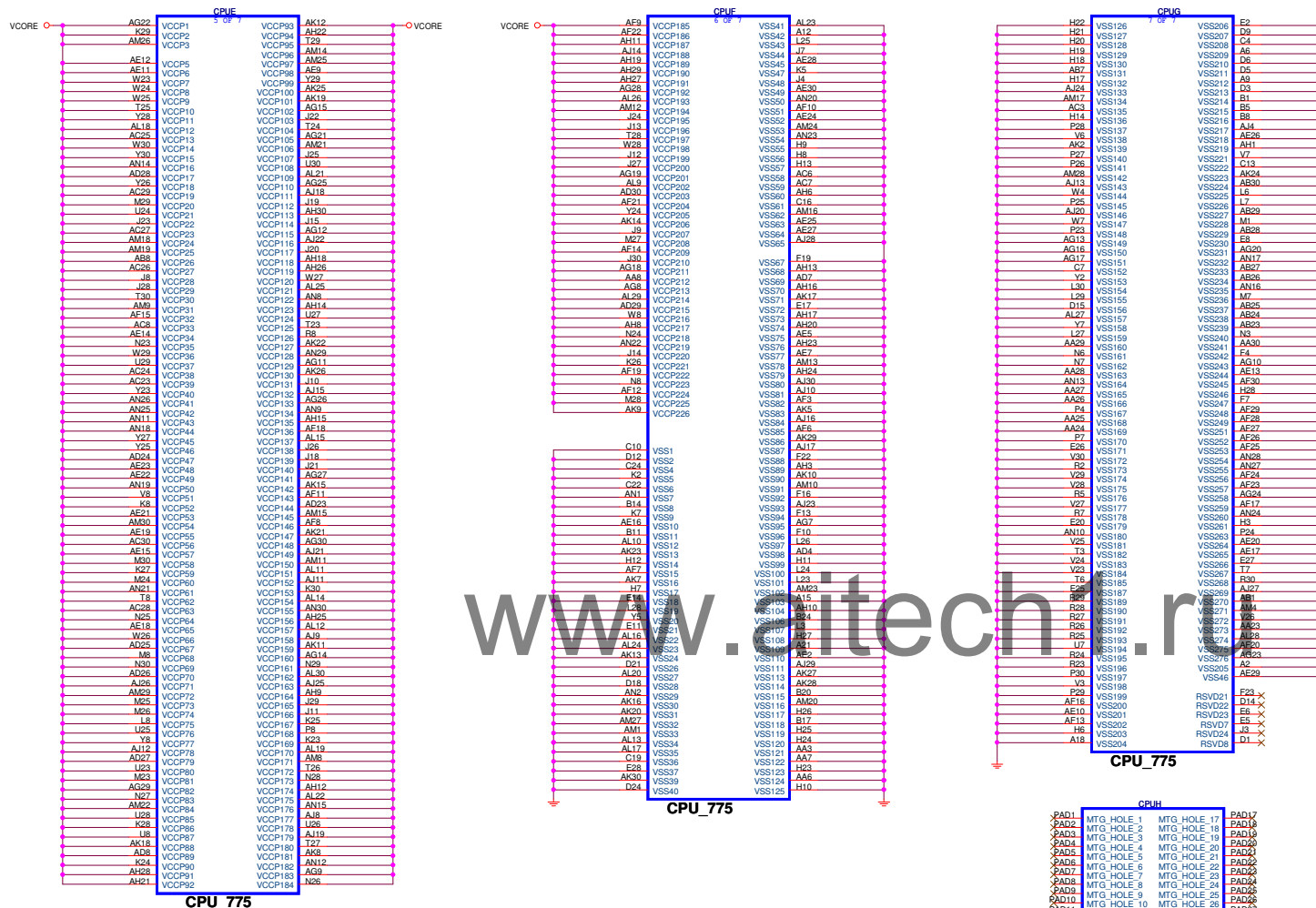
CAN BE EMPTIED FOR BOARD SUPPORTING COREDUO AND WOLFDALE CPU



First International Computer, Inc.
PTMQ45

CPU LGA775-1

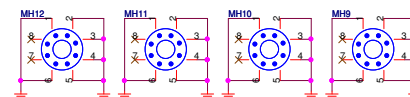
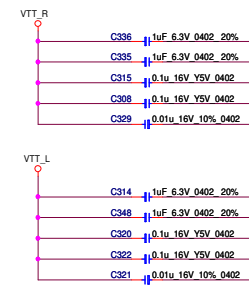
Size C	Document Number D0920E	Rev 1.0
Date:	Monday, August 24, 2009	Sheet 4 of 28

CPU LGA775-2

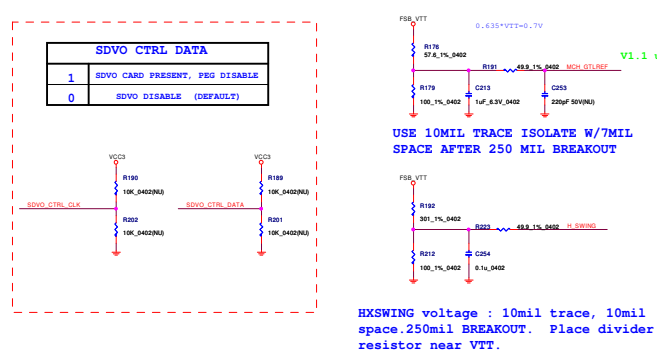
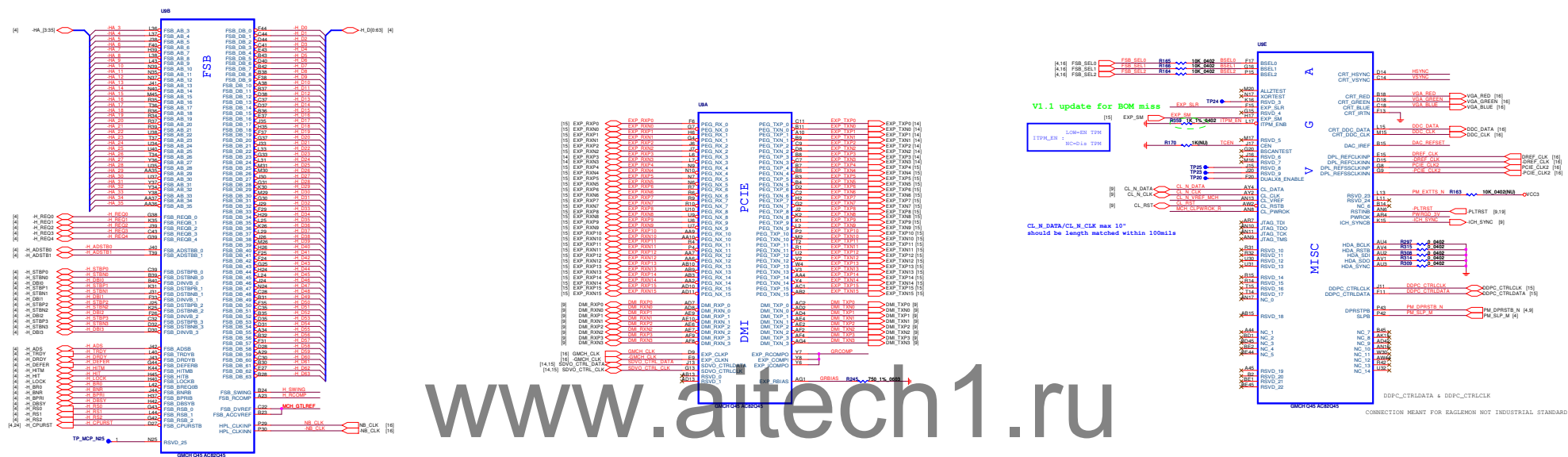
**CAD NOTE: PLACE AS MANY 1206
CAPACITORS AS
POSSIBLE WITHIN CPU CAVITY**

THESE CAPS GO INSIDE CPU CAVITY

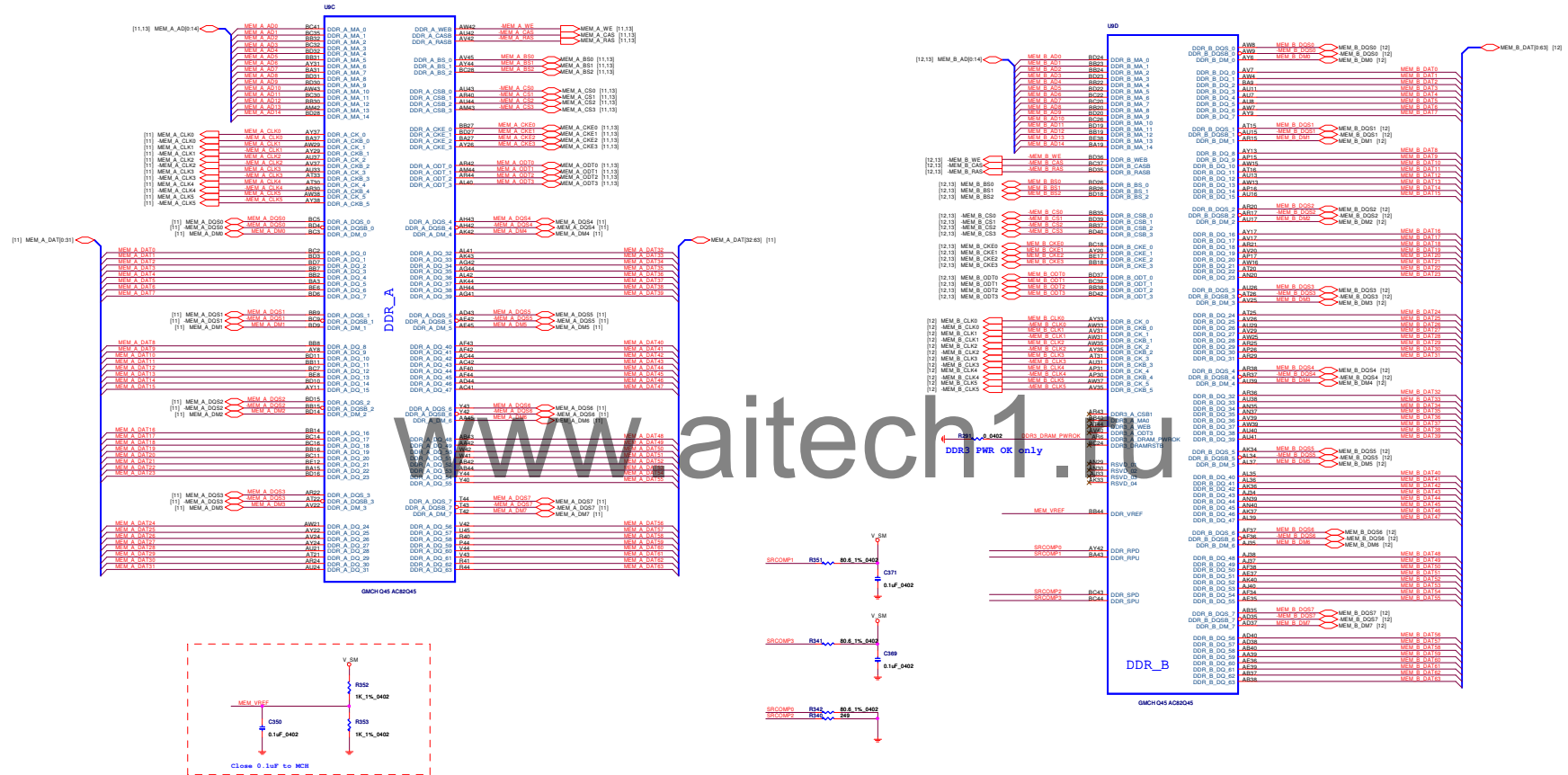
PLACEMENT NOTE FOR 1206:
PLACE 18 INSIDE CPU
SOCKET



EAGLELAKE
GMCH-1



EAGLELAKE GMCH-2



EAGLELAKE GMCH-3

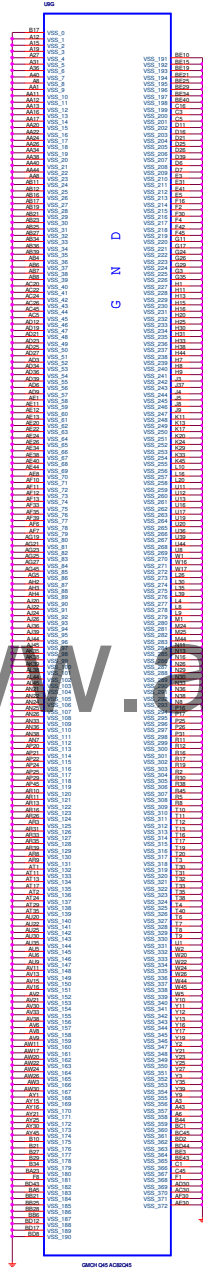
Place in back side for test
V_IPI_C0RE → R017 0.1% 0.000001 0V_IPI_C0L_MCH

UP



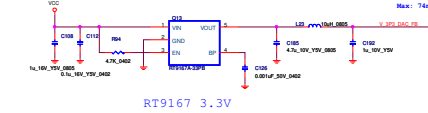
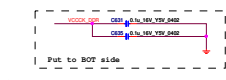
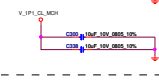
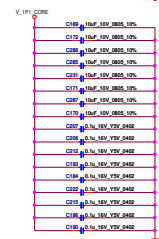
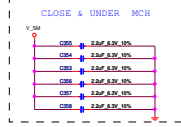
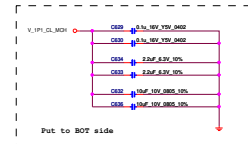
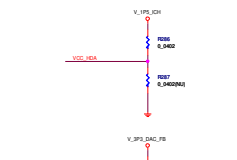
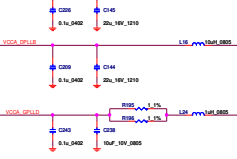
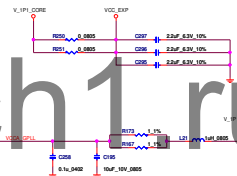
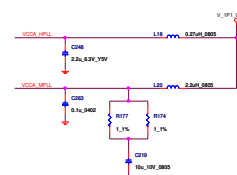
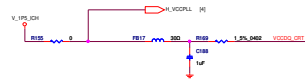
POWER

GMCH-018-03000



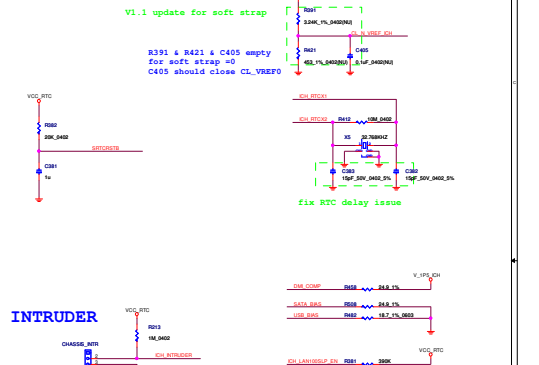
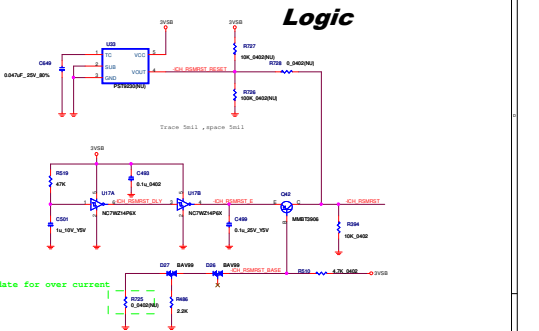
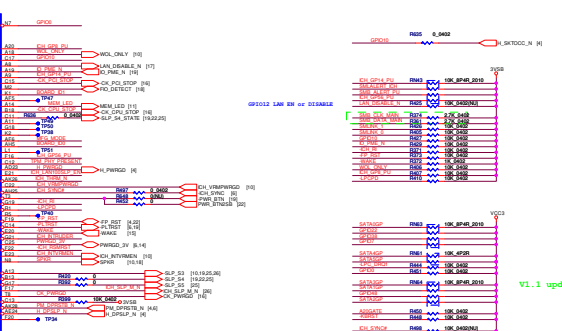
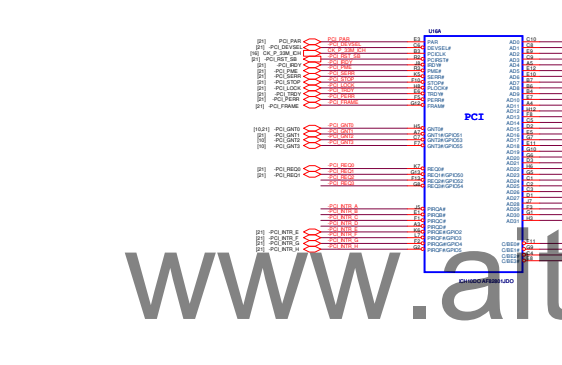
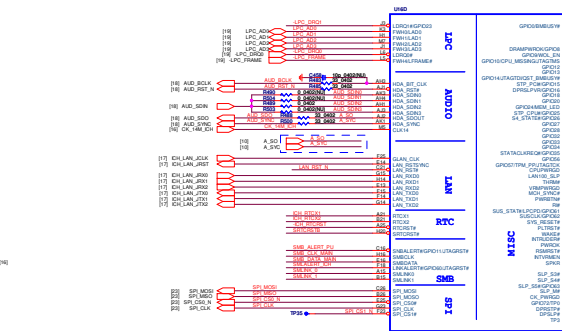
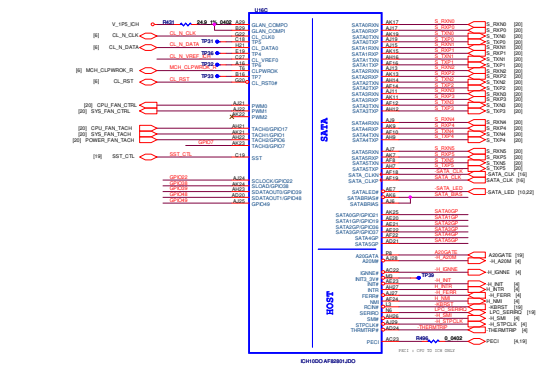
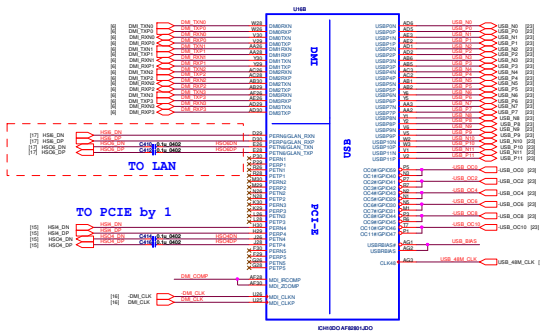
GND

GMCH-018-03000

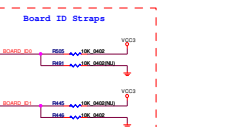
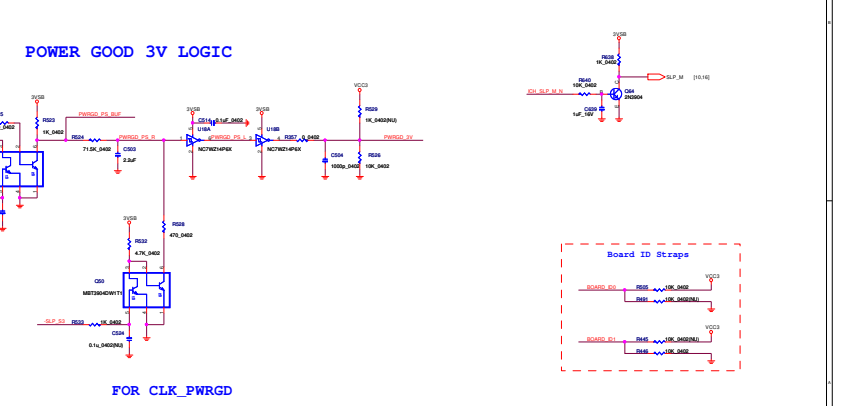
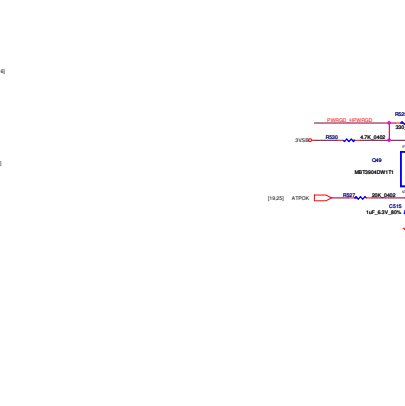
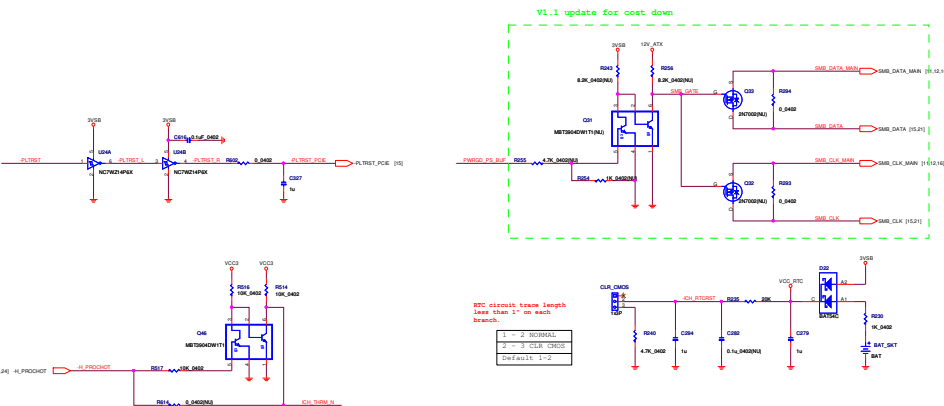


RT9167 3.3V

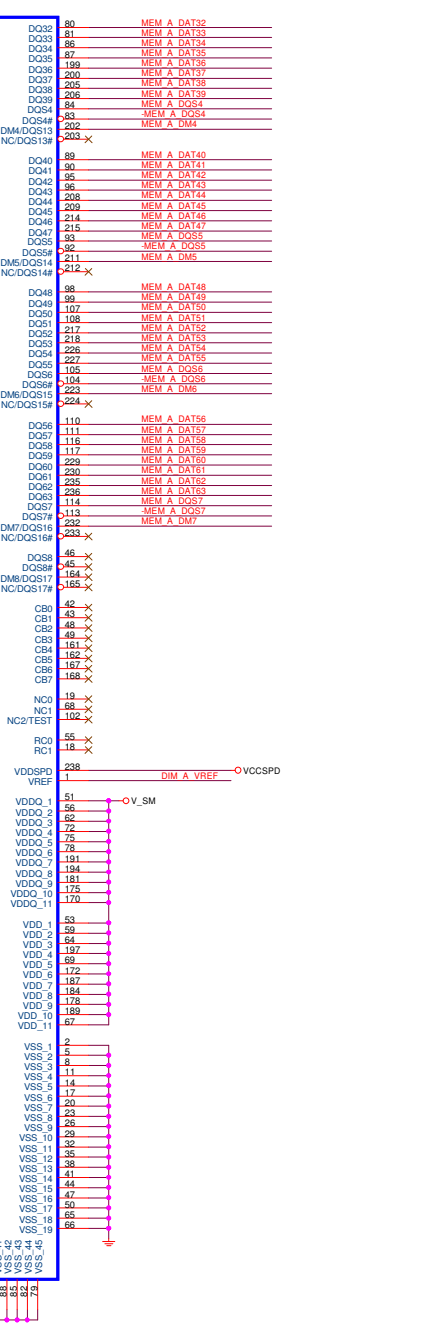
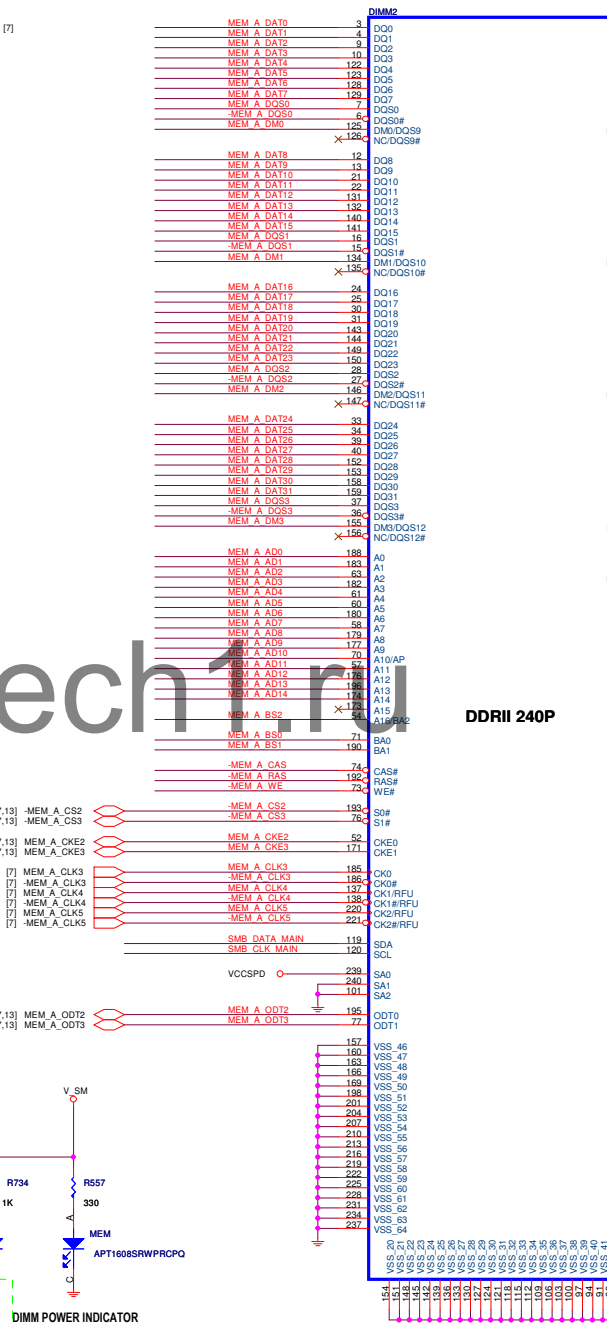
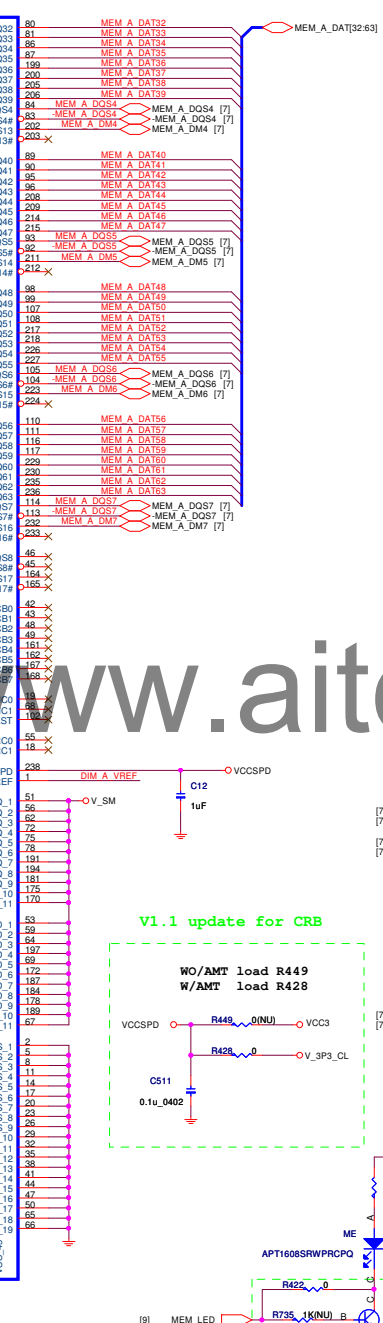
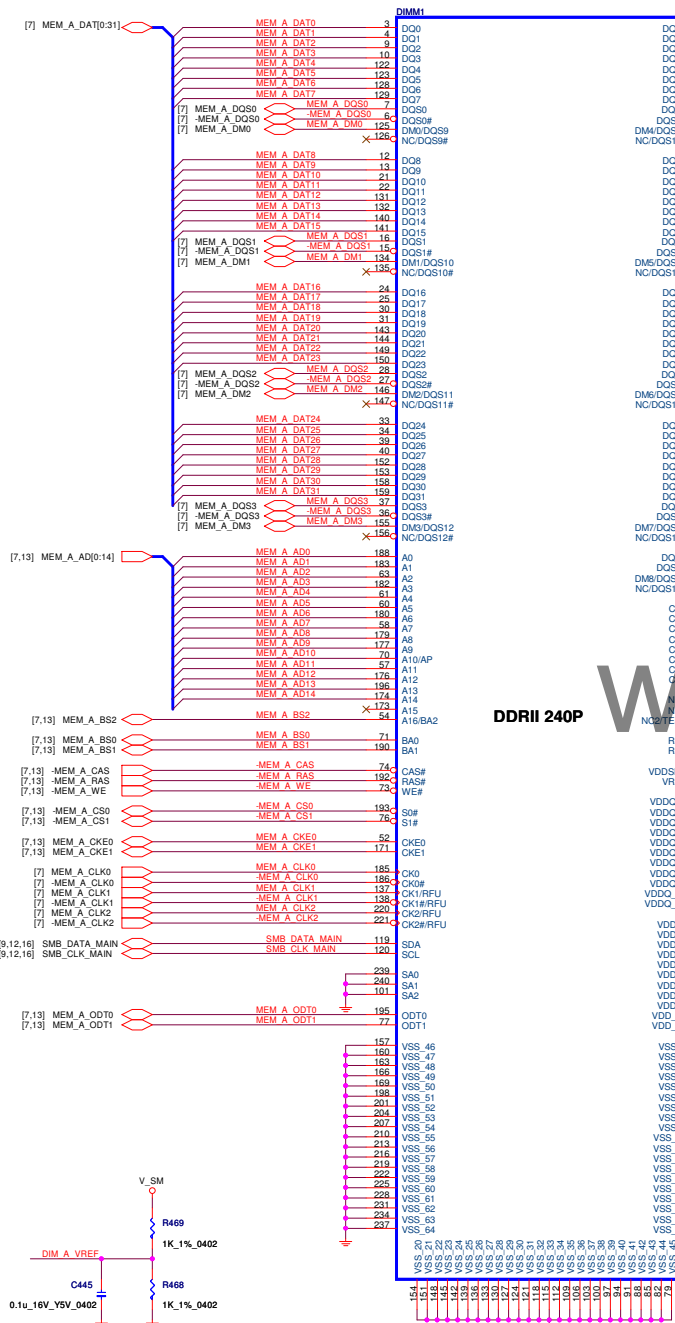
Resume Reset Logic



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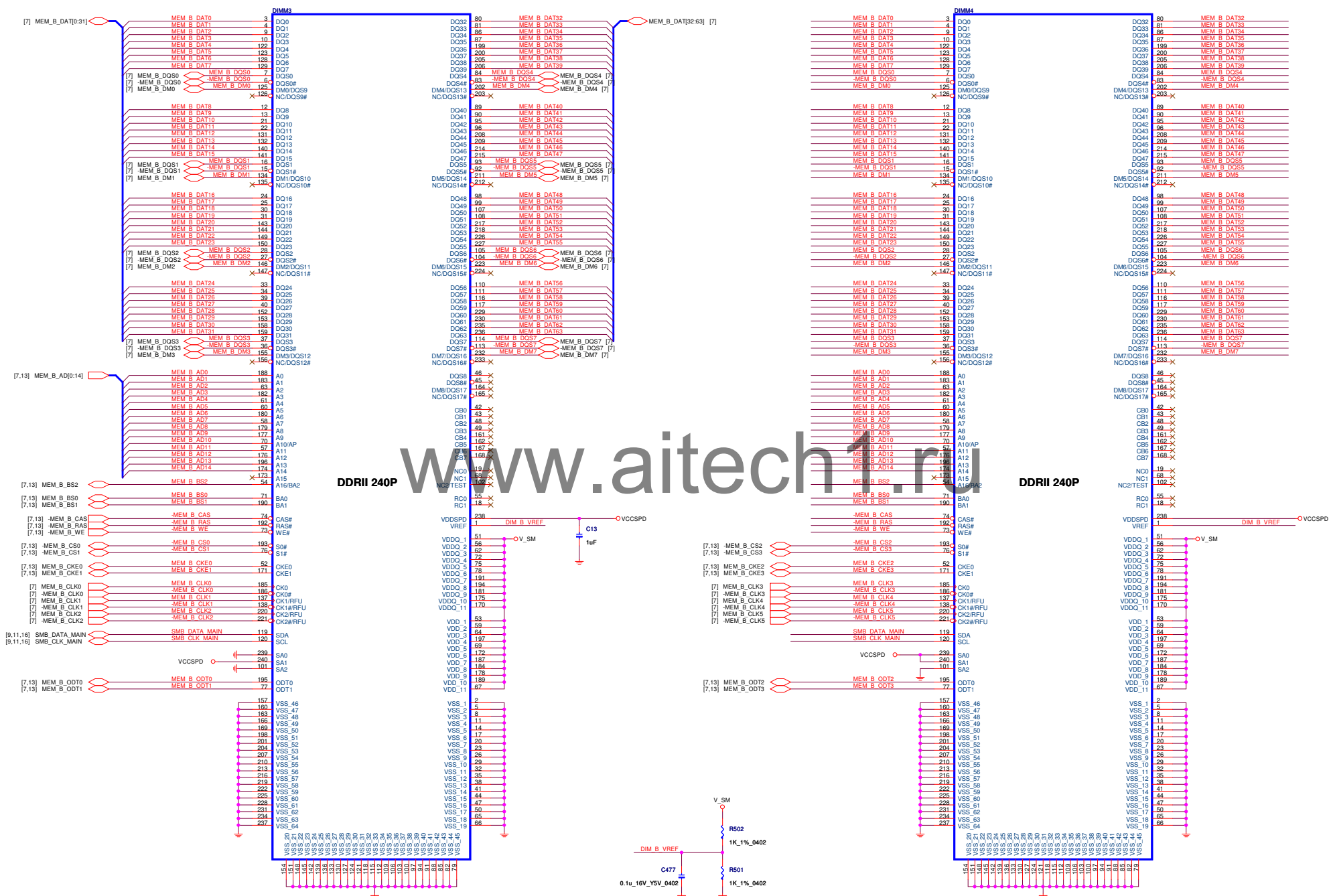
DDR2 CHANNEL-A



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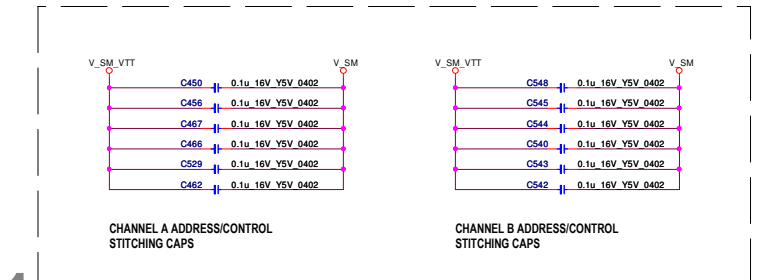
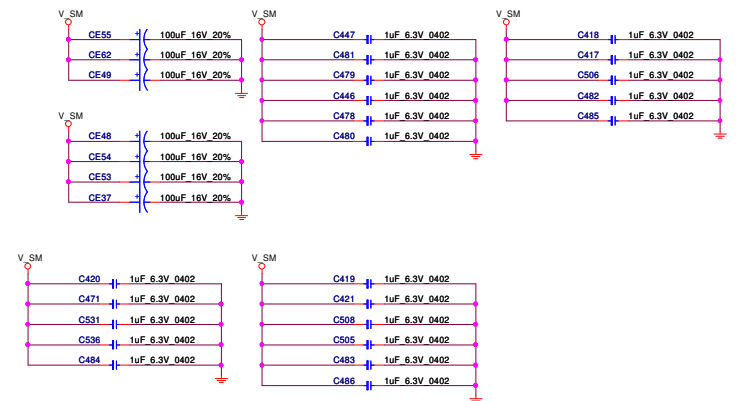
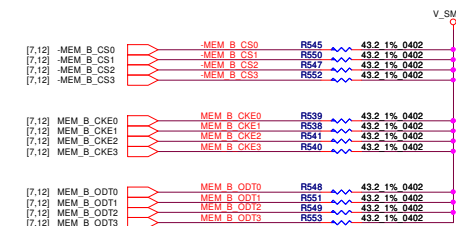
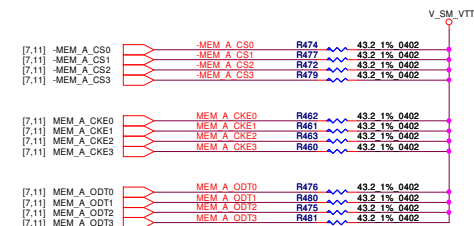
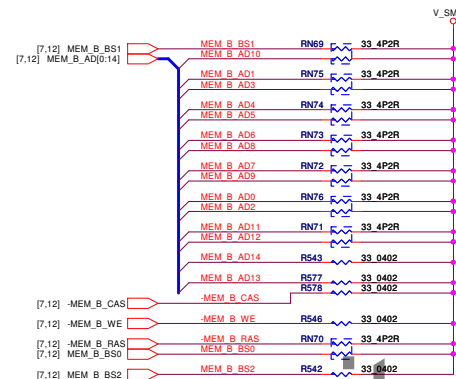
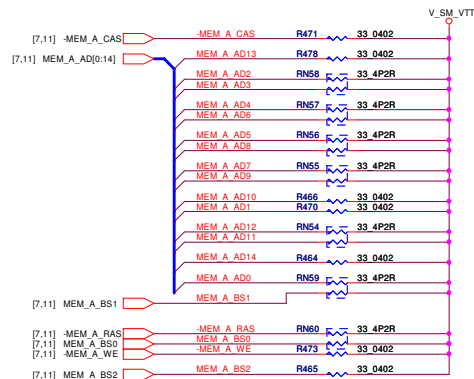
Place components as close as possible to DIMM socket

DDR2 CHANNEL B

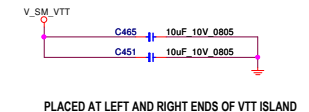
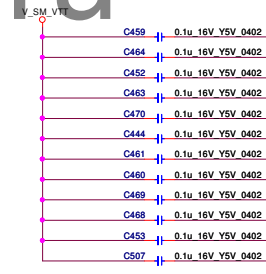


Place components as close as possible to DIMM socket

DDR2 Termination & Decoupling

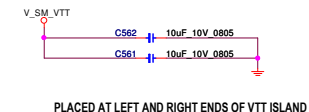
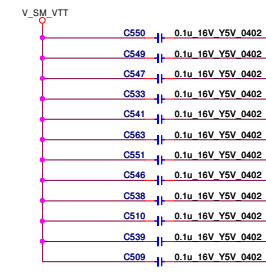


CHANNEL A VTT_DDR DECUPLING CAPS

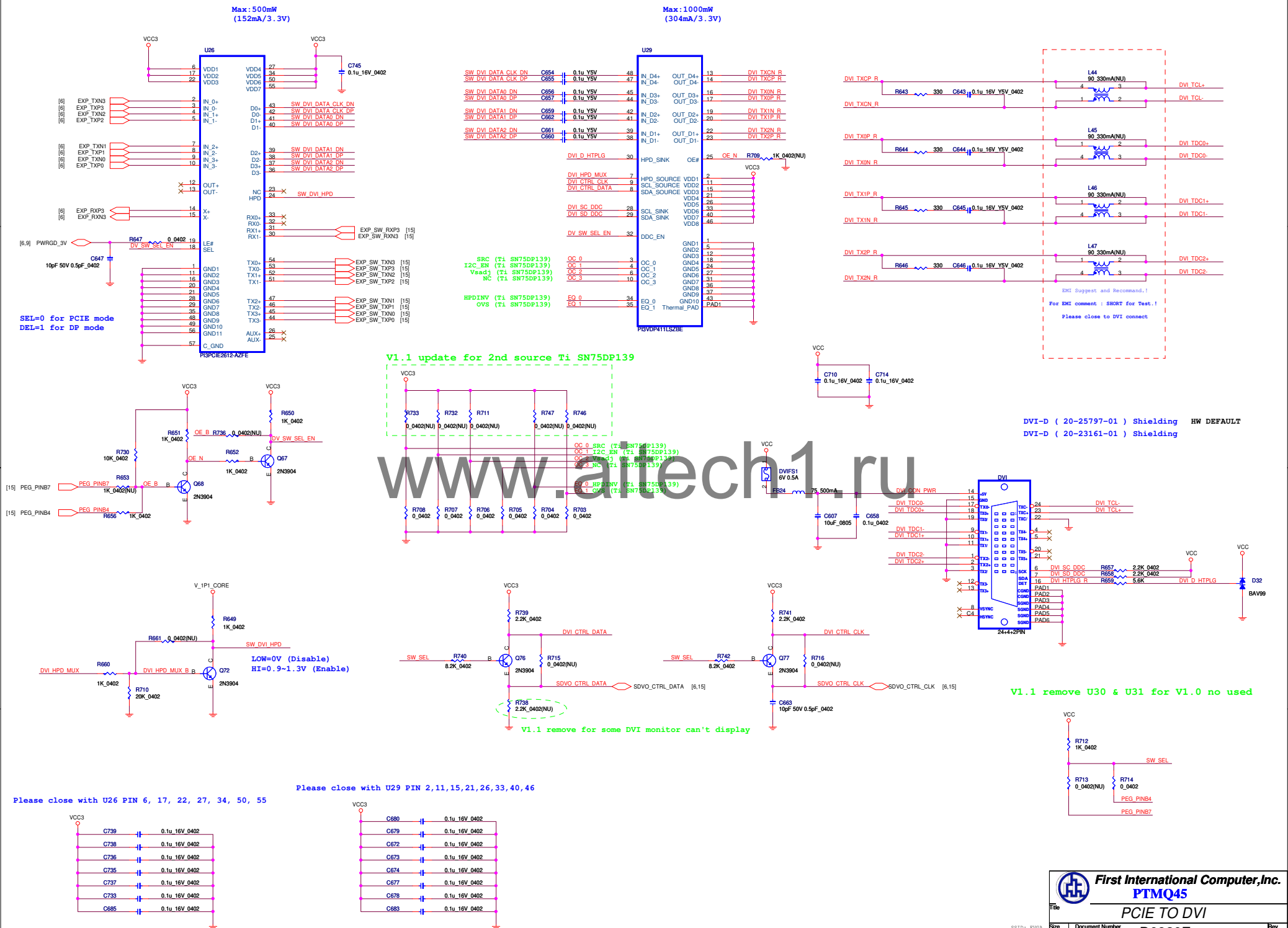


PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND

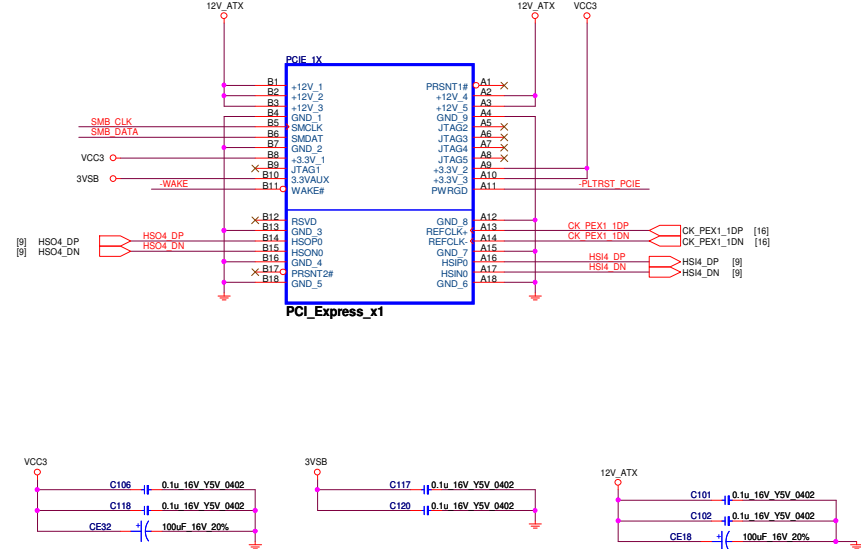
CHANNEL B VTT_DDR DECUPLING CAPS

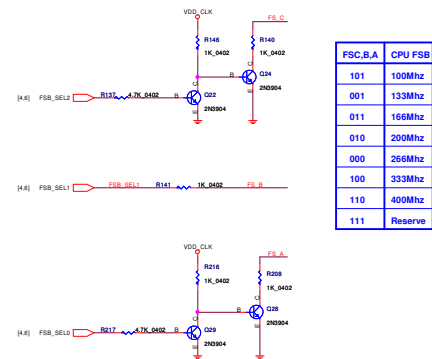


PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND

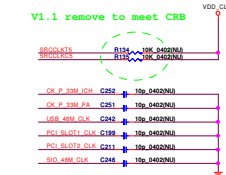
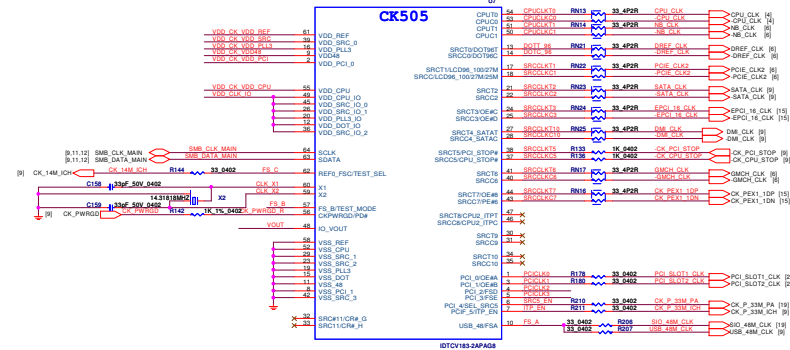


PCI EXPRESS x1

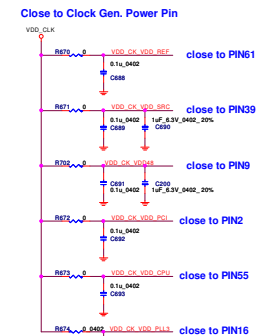


CLOCK GEN.

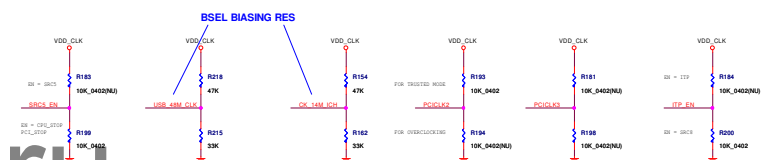
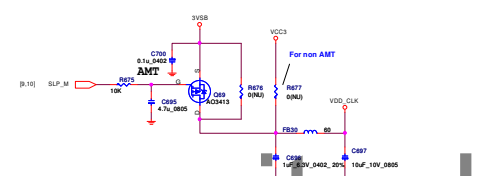
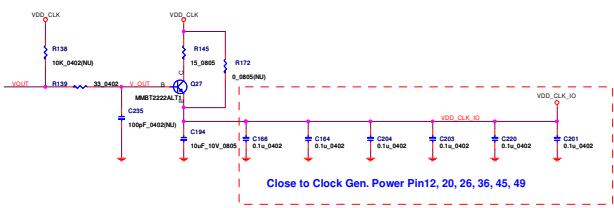
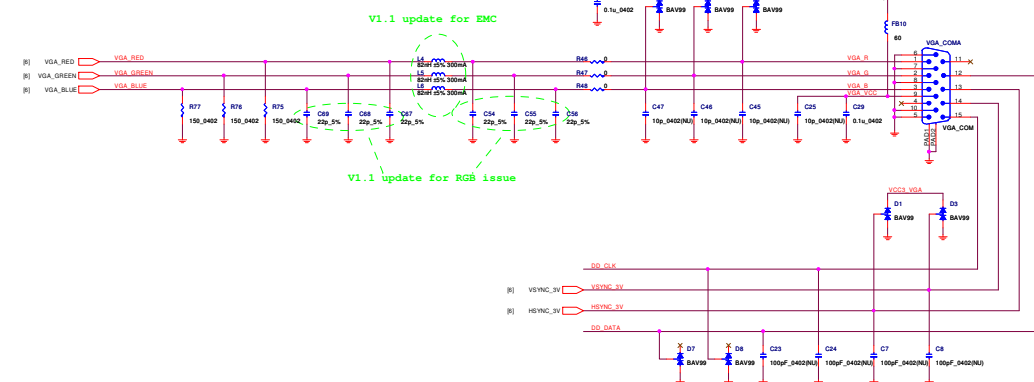
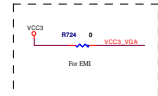
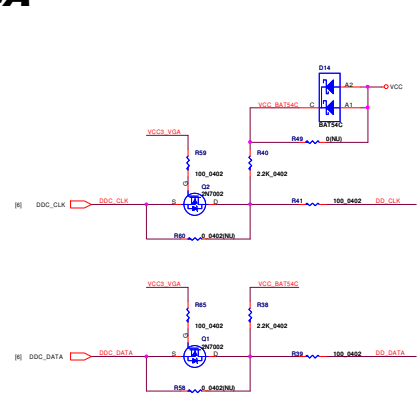
FSC,B,A	CPU FSB
101	100Mhz
001	133Mhz
011	166Mhz
010	200Mhz
000	266Mhz
100	333Mhz
110	400Mhz
111	Reserve



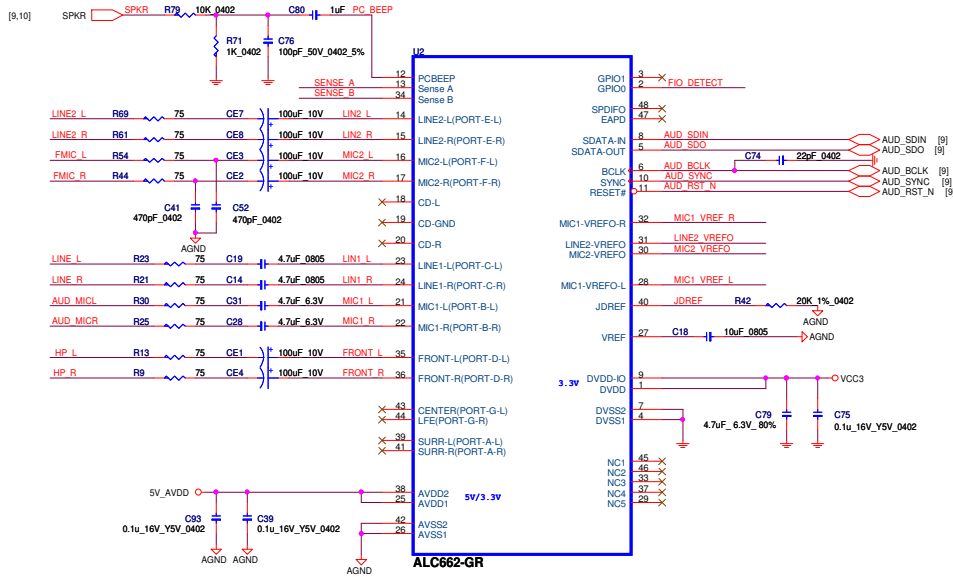
PCICLK2	0=overclock allow; 1=overclock not allow
SRC5_EN	(PIN37,38) 0=CPU_STOP,PCI_STOP for AMT; 1= SRC5
IPT_EN	(PIN46,47) 0=SRC8; 1=ITP



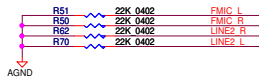
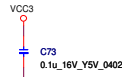
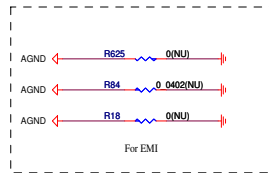
PINS,PIN#	DPGT,C2PG (pin1, pin2)	N program enable	CPU	SATA PIN17,22	PCI	PIN17,18	SRC	48/96
Low,0	0,0	1	PLL1	PLL4 SRC	PLL4	CFB table	PLL4	PLL2
Low,1	0,0	0						
Mid,0	0,1	1	PLL1	PLL3	PLL3	CFB table	PLL4	PLL2
Mid,1	0,1	0						
High,0	1,0	1	PLL1	PLL3	PLL3	CFB table	PLL4	PLL2
High,1	1,1	1	PLL1	PLL4	PLL4	Pin17 SRAM, PLL2 Pin18 T3MA PLL3	PLL4	PLL2

**VGA**

AC97_ALC662

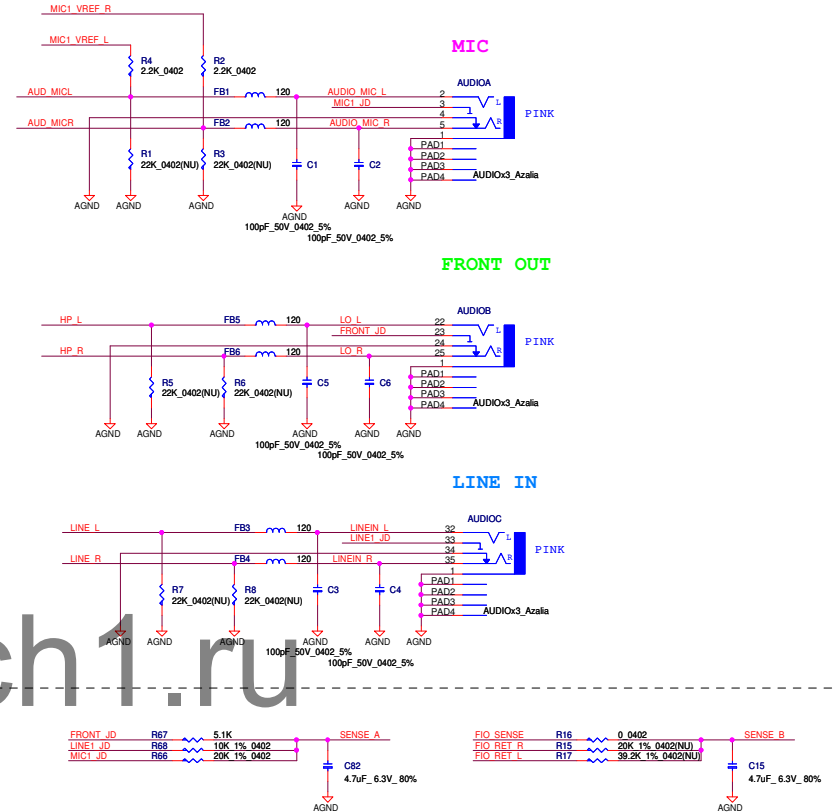


ALC662-GR



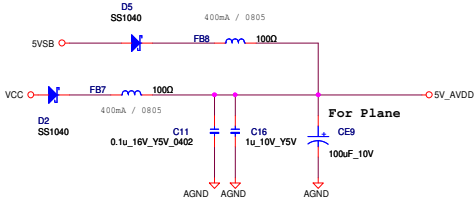
SSID: AUC

Rear Audio Connector



SSID: AUC

5V_AVDD



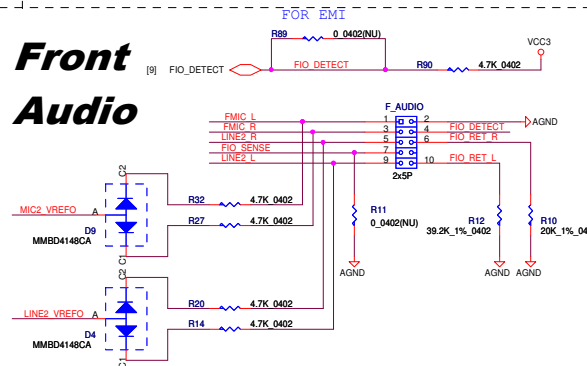
SSID: AUC

Isolation



Please place to BOT side

Front Audio



SSID: AUC

Azalia Jack Sense Network

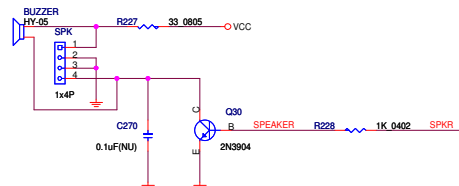
Jack Sense A	Jack Sense B
5K Rear I/O Front Out	20K Front I/O MIC IN
10K Rear I/O Line IN	39K Front I/O HP IN
20K Rear I/O MIC IN	

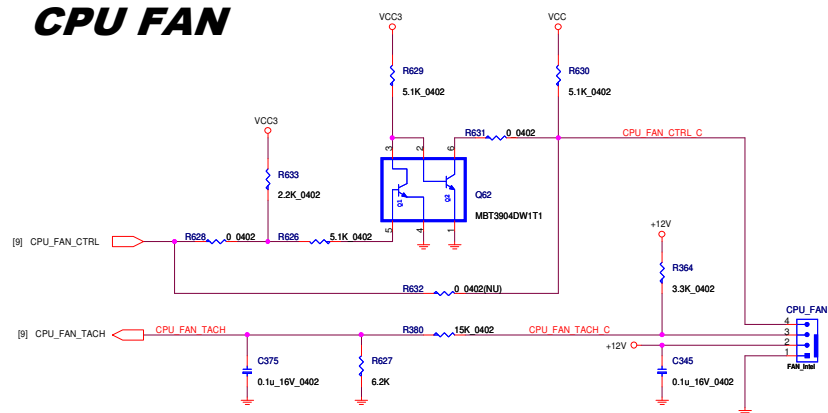
AUDIO CONNECTOR

REAR IO AUDIO CONNECTOR PLACEMENT

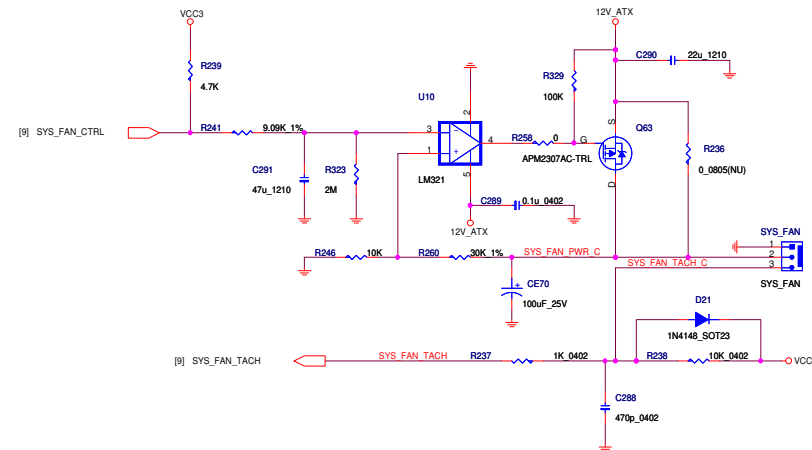
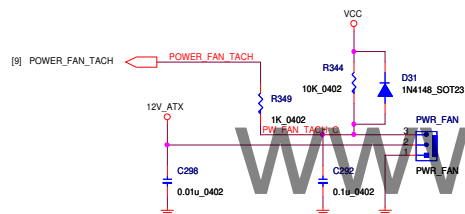
LINE IN
FRONT OUT
MIC

Speaker

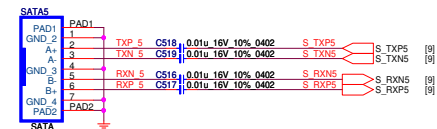
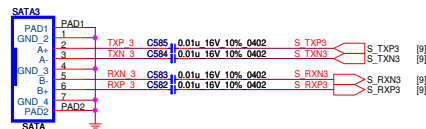
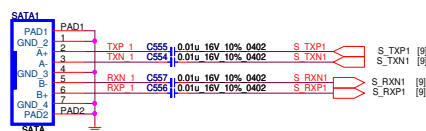
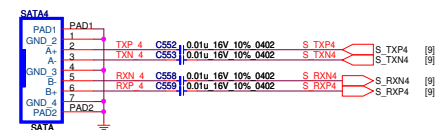
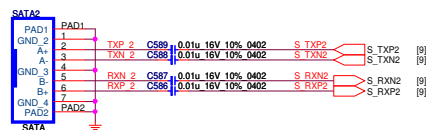
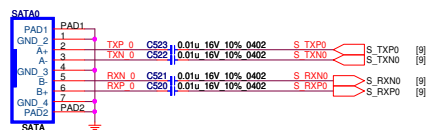


CPU FAN

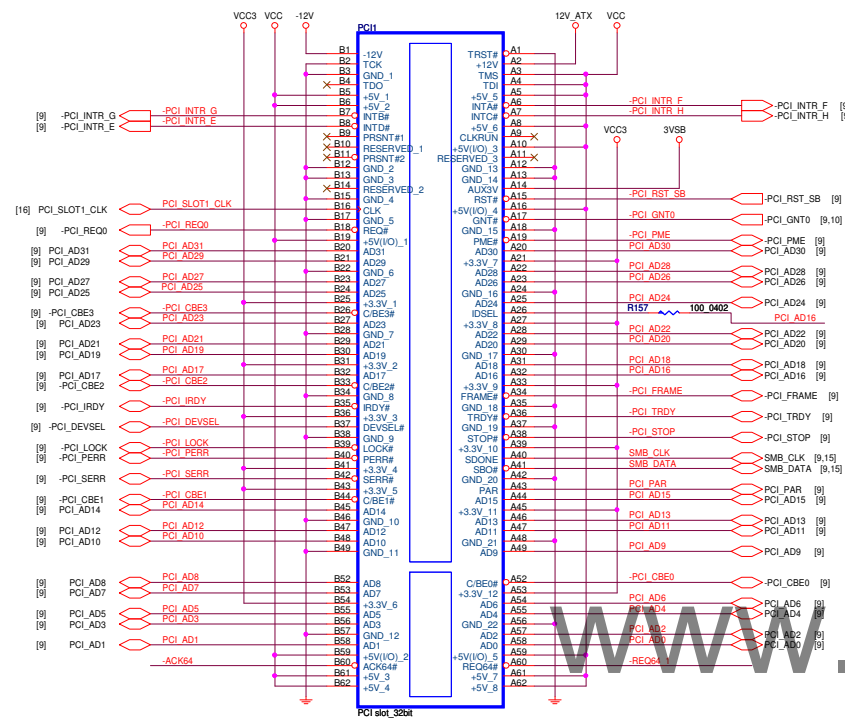
System FAN

**Power FAN**

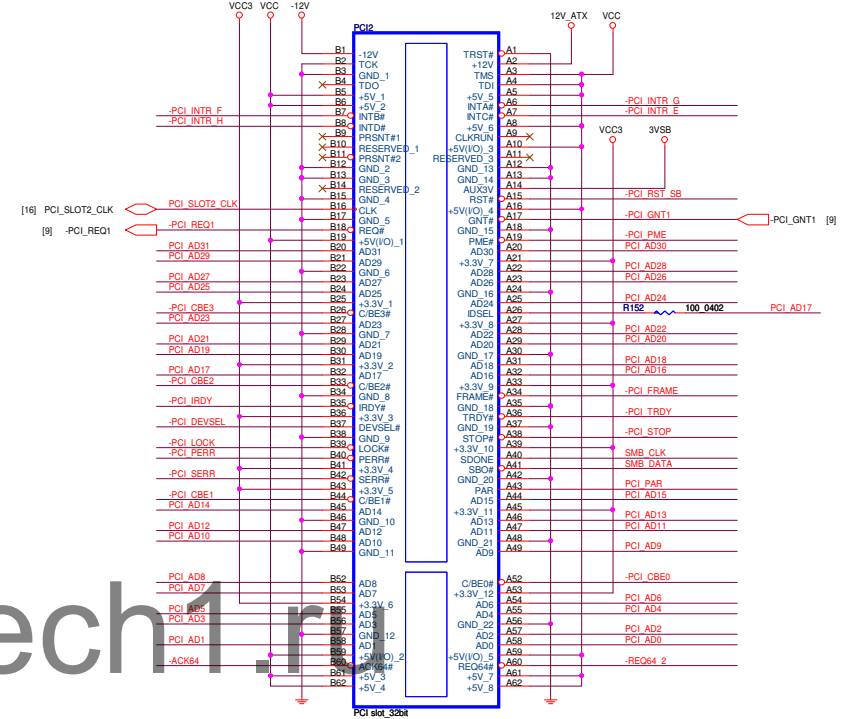
SATA



PCI SLOT 1, 2

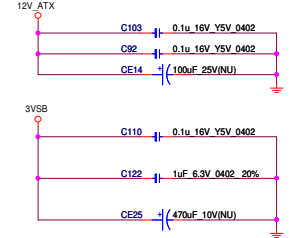
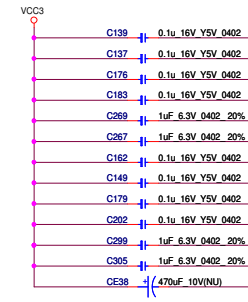
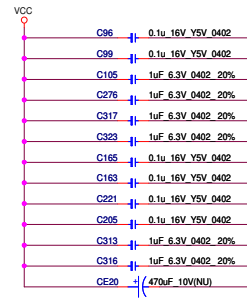


-INTR_A: -INTR_F
-INTR_B: -INTR_G
-INTR_C: -INTR_H
-INTR_D: -INTR_E
IDSEL: AD16
REQ/GNT: 0

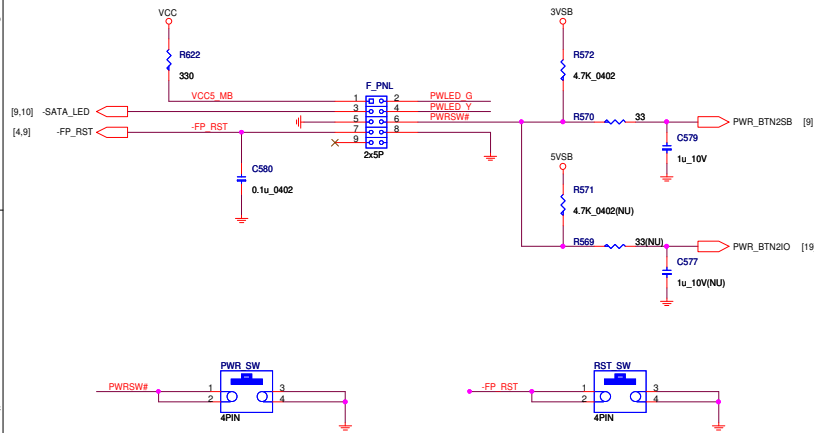


-INTR_A: -INTR_G
-INTR_B: -INTR_F
-INTR_C: -INTR_E
-INTR_D: -INTR_H
IDSEL: AD17
REQ/GNT: 1

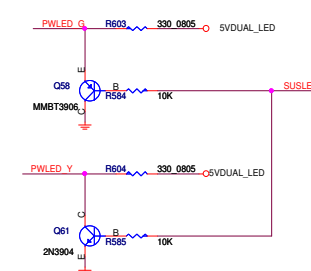
PCI Decoupling



Front Panel

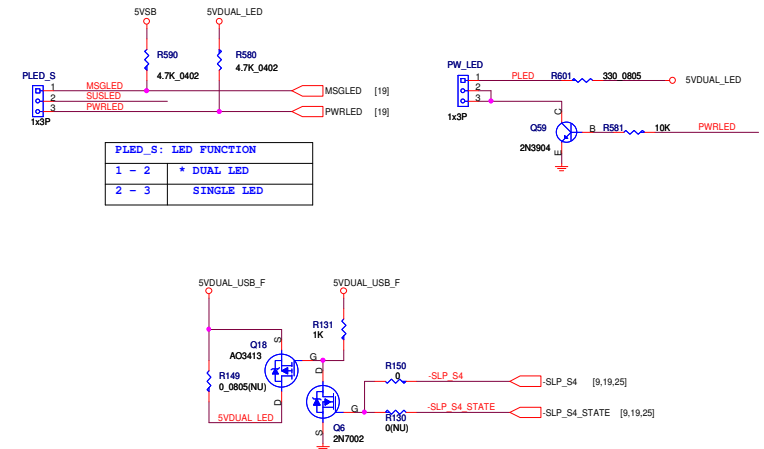


Suspend LED



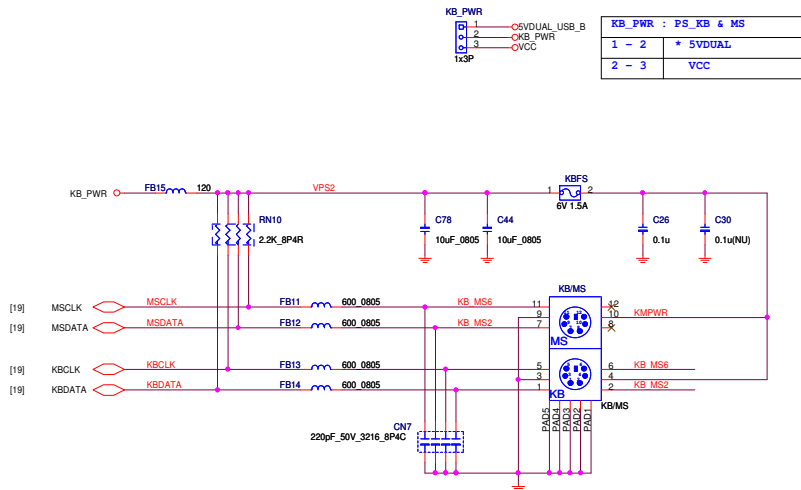
LED STATUS	S0	S1/S3	S4	S5
GREEN LED	ON	OFF	OFF	OFF
YELLOW LED	OFF	ON	OFF	OFF
PW_LED	ON	BLINKING	OFF	OFF

Power LED



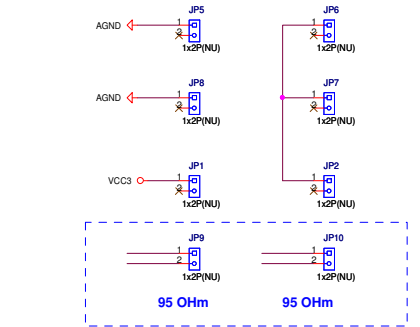
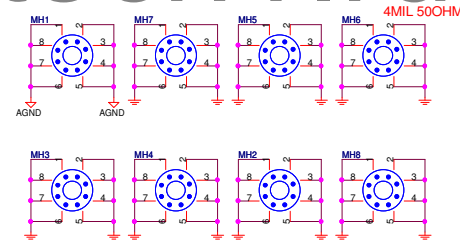
PLED_S: LED FUNCTION	
1 - 2	* DUAL LED
2 - 3	SINGLE LED

PS2_KB/MS

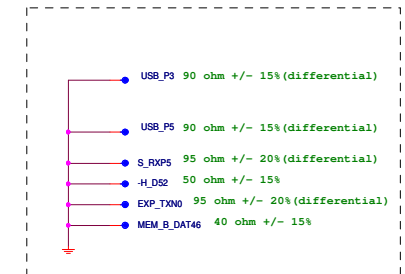


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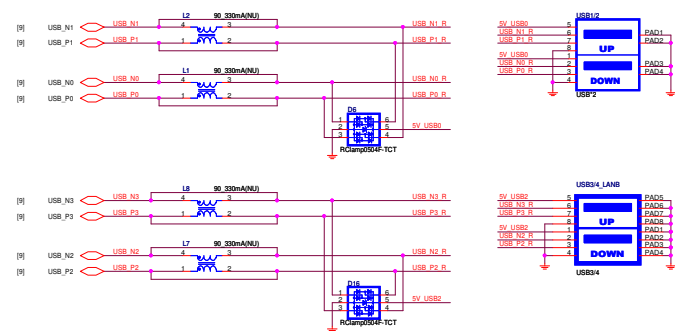
Mount Hole



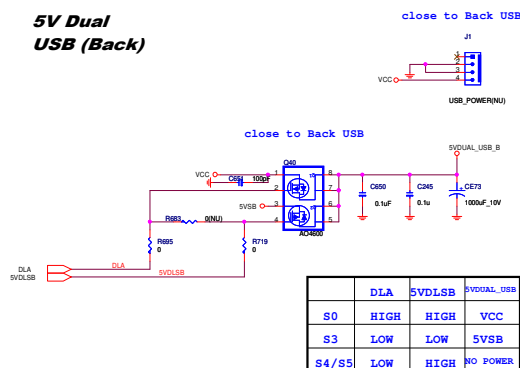
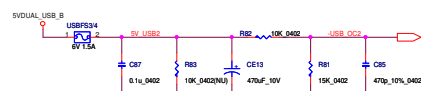
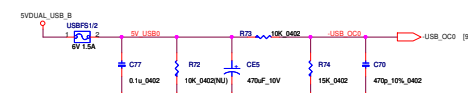
Impedance test point



USB(Rear Connectors)

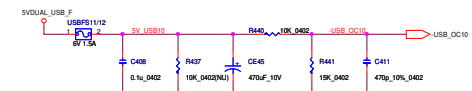
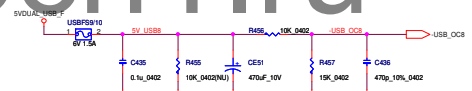
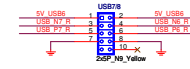
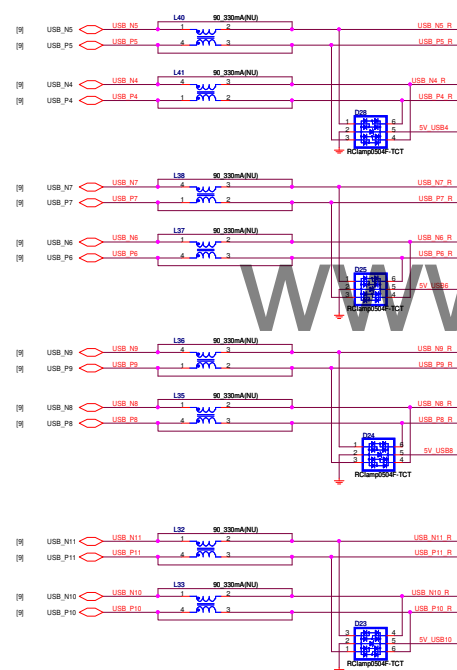


**5V Dual
USB (Back)**

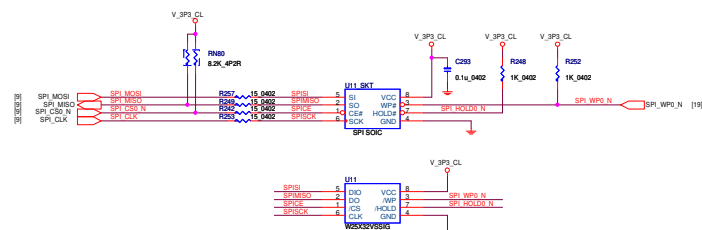


	DLA	5VDLSB	5VDUAL
S0	HIGH	HIGH	VCC
S3	LOW	LOW	5VSB
S4/S5	LOW	HIGH	NO POWER

USB (Front Connectors)

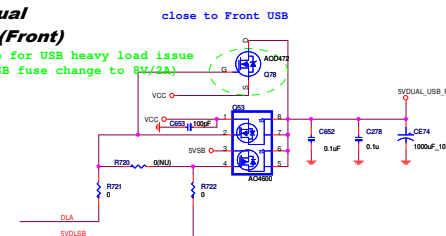


SPI Flash



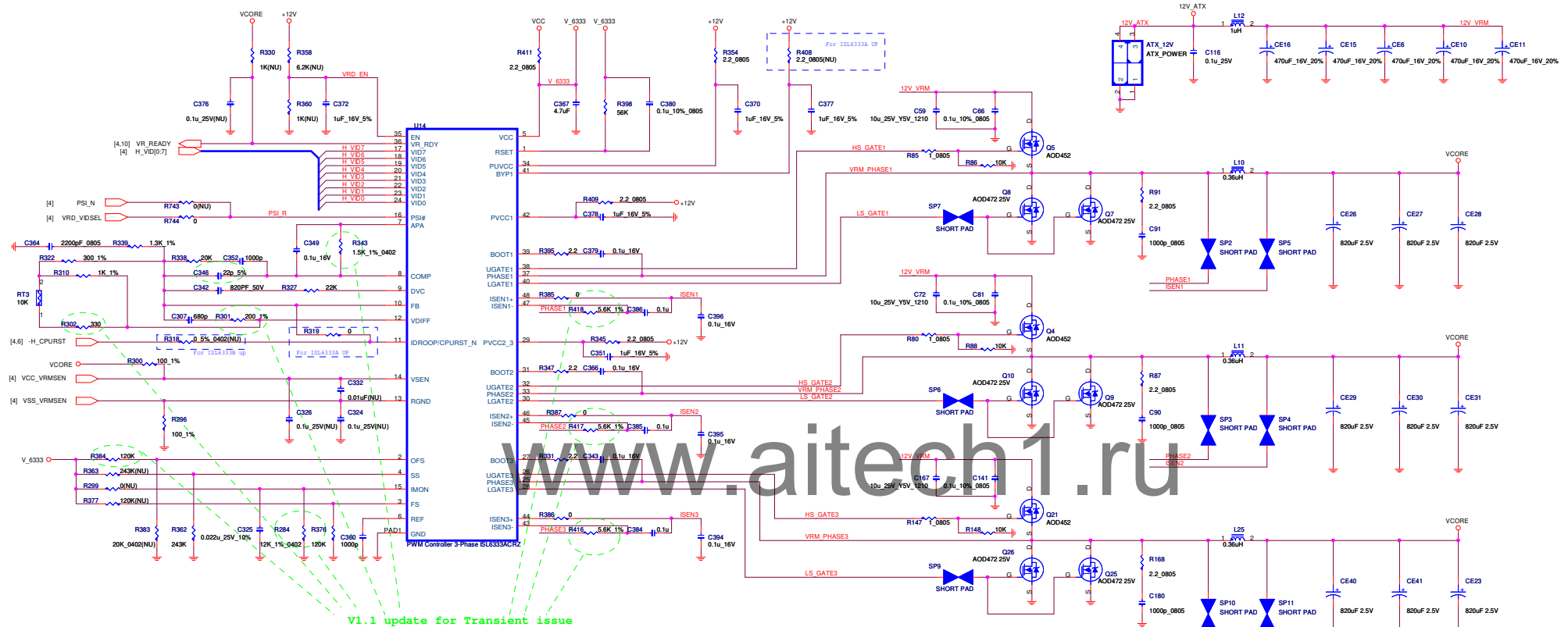
**5V Dual
USB (Front)**

V1.1 update for USB heavy load issue
(include USB fuse change to 8V/2A)

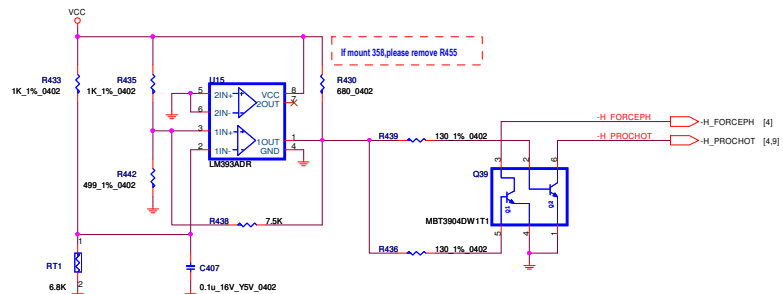


	DLA	5VDLSB	5VDUAL
S0	HIGH	HIGH	VCC
S3	LOW	LOW	5VSB
S4/S5	LOW	HIGH	NO POWER

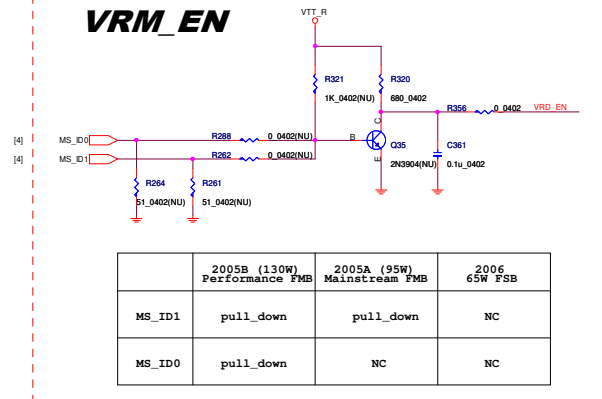
VRM(ISL6333A_CRZ)



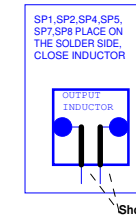
VRM Thermal Monitor



VRM_EN

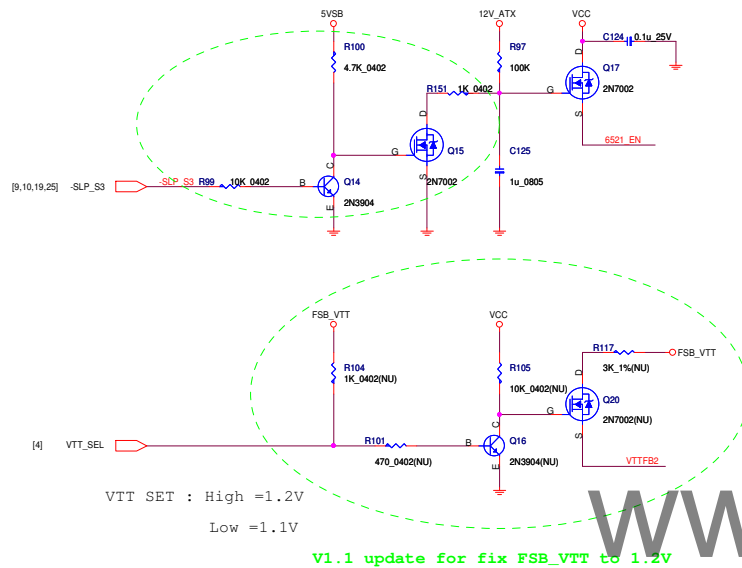


	2005B (130W) Performance FMB	2005A (95W) Mainstream FMB	2006 65W FSB
MS_ID1	pull_down	pull_down	NC
MS_ID0	pull_down	NC	NC

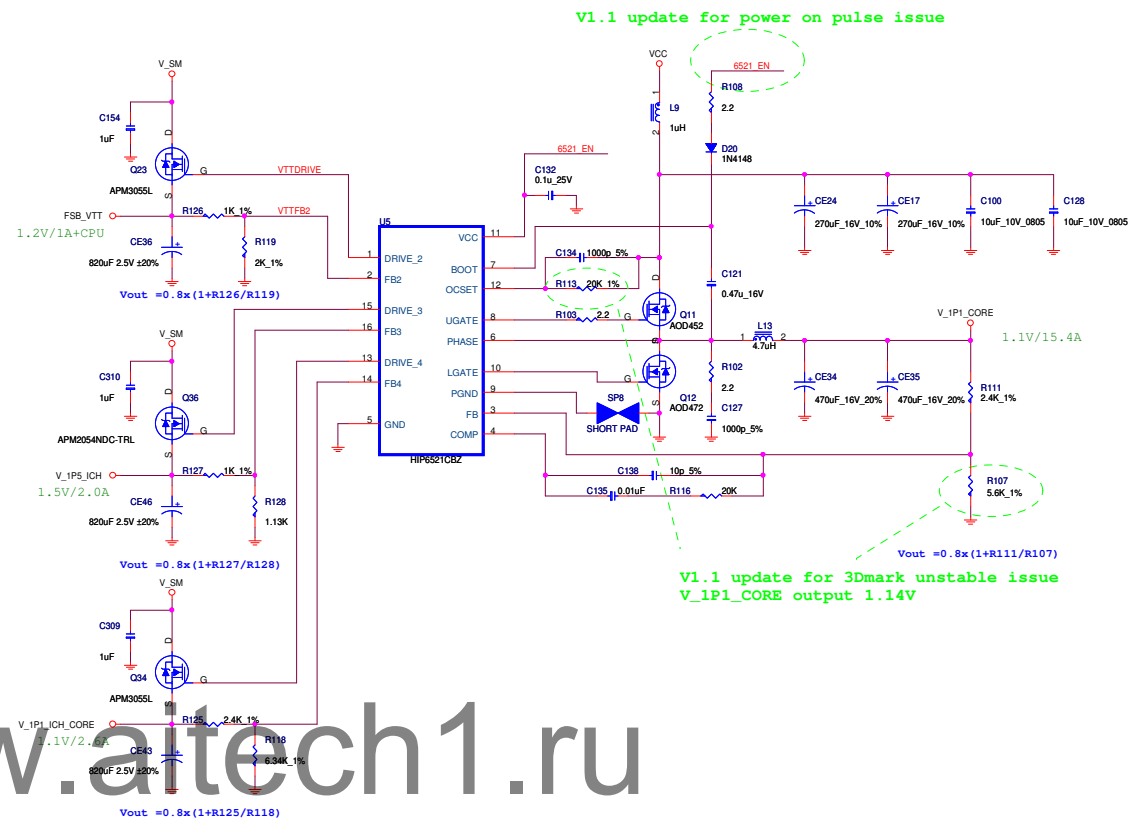


**SYSTEM
POWER**

V1.1 update for power on delay

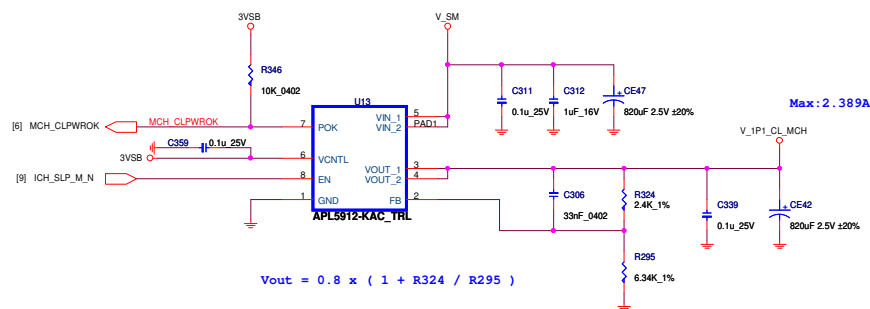


V1.1 update for fix FSB_VTT to 1.2V



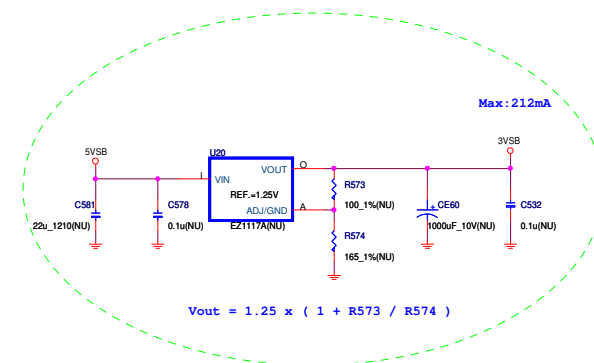
```
V1.1 update for 3Dmark unstable issue
V_1P1_CORE output 1.14V
```

V_1P1_CL_MCH
(1.1V)

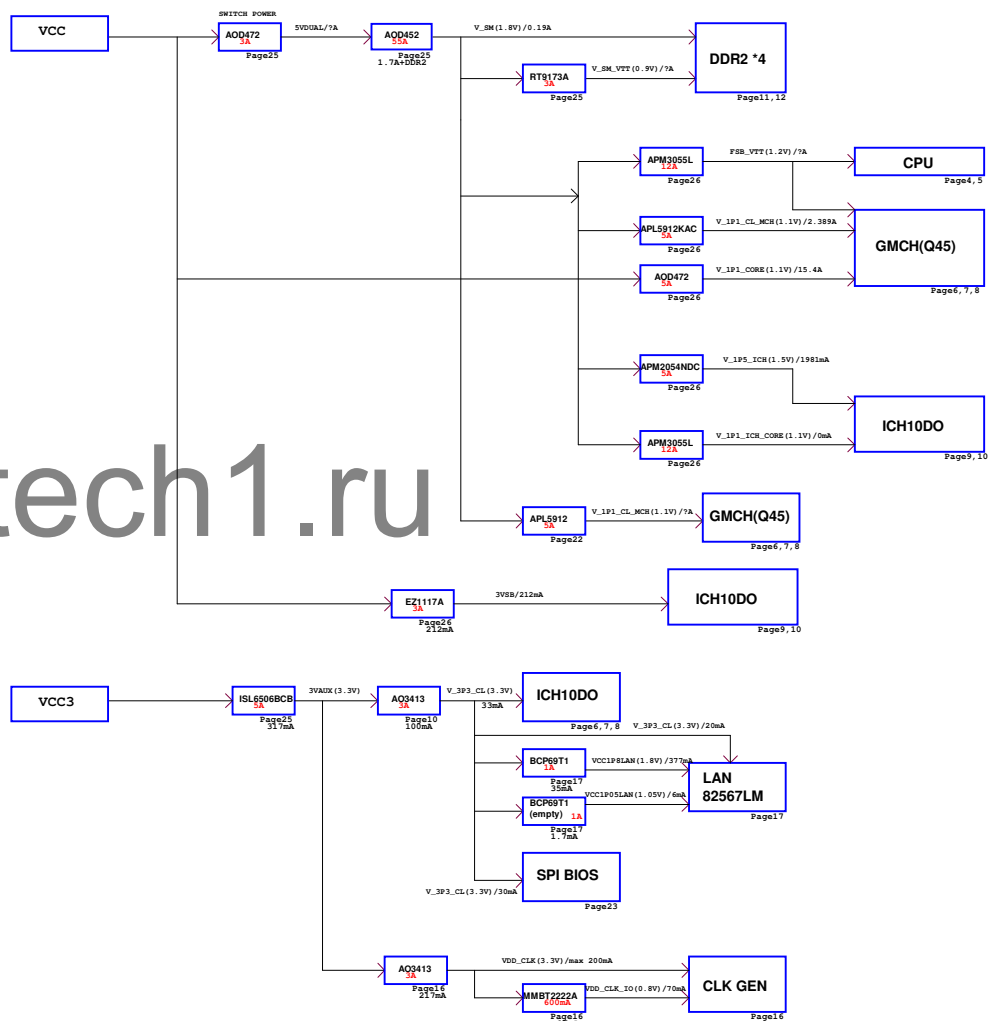

$$V_{out} = 0.8 \times (1 + R_{324} / R_{295})$$

3VSB For SB

V1.1 update for cost down


$$V_{out} = 1.25 \times (1 + R_{573} / R_{574})$$

ME (M0 state) Power Diagram



PTMQ45 POWER Rail

Power	Description	Voltage	Type	Max	Max Total	Source (ESTIMATED)
1V	VR Vcc1p0_core	1V	5.95A	8.5A	10.514A	VCC/2.103A
1V	VR VccA1p0_DHPLL	1V	0.15A	0.4A		
1V	VR VccA1p0_DPLL	1V	0.1A	0.2A		
1V	VR VccA1p0_AHPLL	1V	0.1A	0.2A		
1V	VR VccA1p0_TPL	1V	0.1A	0.2A		
1V	VR Vcc1p0_DDR	1V	0.1A	1A		
1V	ICH10 V-CPU-IO	1V		1mA		
1.1V	ICH10(core/sus)	1.1v		2.553A	2.553A	VCC/0.56A
1.1V	VR Vcc1p2_LCIA	800MHZ	3.02A	4.31A	4.71A	VCC/1.036A
1.1V	VR Vcc1p2_IOPLL_LCIA	1.1V	0.1A	0.2A		
1.1V	VR Vcc1p2_COREPLL_LCIA	1.1V	0.1A	0.2A		
1.2V	FSB_VTT	1.2V	418mA	914mA	0.914A	V_SM/610mA
1.25V	VR VccA1p25_DPLL_DMI	1.25V	0.1A	0.2A	0.6A	V1.5/0.5A
1.25V	VR VccA1p25_APLL_DMI	1.25V	0.1A	0.2A		
1.25V	VR VccA1p25_RXTX_DMI	1.25V	0.1A	0.2A		
1.5V	ICH10 Vcc1.5A	1.5V		1.39A	2078mA	V_SM/1731mA
1.5V	ICH10 Vcc1.5B	1.5V		591mA		
1.5V	ICH10 V1.5 USBPLL	1.5V		10mA		
1.5V	ICH10 V1.5 DMIPLL	1.5V		22mA		
1.5V	ICH10 V1.5 SATAPLL	1.5V		42mA		
1.5V	ICH10 V1.5 GLANPLL	1.5V		23mA		
1.5V	V_1P5_ICH	1.5V		1981mA	1981mA	V_SM/1651mA
1.8V	LAN VDD1P8--825671M	1.8V		377mA	377mA	V_3P3_CL/206mA
VCC3	VR VccA3P3_BG_DMI	3.3V	0.4mA	0.7mA	2.851A	VCC3/2.851A
VCC3	VR VccA3P3	3.3V	0.715A	1.78A		
VCC3	ICH10 Vcc3	3.3V		273mA		
VCC3	CLOCK_IC595410	3.3V	300mA	500mA		
VCC3	ICH7 VccRTC	3.3V		G3.6uA		
VCC3	LAN VDD3.3-82541I	3.3V		148mA		
VCC3	NET2280	3.3V		92mA		
VCC3	ICH10 VCC_3P3_CL	3.3V		70mA		
VCC3	ICH10 V_AZCORE	3.3V		30mA		
3VSB	ICH10 VccSUS_HDA	3.3V		31mA	52mA	5VSB/0.03432A
3VSB	ICH10 VccSUS3.3	3.3V		212mA		
VCC	SATA_HDD_CON	5V		700mA	2696.7mA	VCC/2.6967A
VCC	VR VccA5p0_EXP	5V	0.7mA	23.4mA		
VCC	VR VccA5P0_PER	5V	0.7mA	17.3mA		
VCC	APW7120	5V		6mA		
VCC	ISL6545*2	5V		100mA		
VCC	USB_VCC*7	5V		1750mA		
VCC	I/O ITE8712	5V		100mA		
+12V	CPU FAN*2	12V		180mA	180mA	12V/0.18A
5VSB	APW1172	5V		12mA	44mA	5VSB/0.044A
5VSB	ICH7 V5REF	5V		6mA		
5VSB	ICH7 V5REF_SUS	5V		10mA		
5VSB	APL1085-3.3	5V		10mA		
5VSB	APW7120	5V		6mA		
1.8V	VR Vcc1p8-DDR	1.8V		3.3A	6.5A+0.045A	VCC/2.356A
1.8V	1p8-DDR-ON BOARD	1.8V		3.2A		
0.9V	DDR2 VTT	0.9V		90mA	90mA	DDR2_1P8/0.045A
5V(TOTAL)				VCC/9.0897A_45.4485W		
VCC3(TOTAL)				VCC3/2.8578A_9.43074W		
12V(TOTAL)				12V/0.18A_2.16W		
5VSB(TOTAL)				5VSB/0.28952A_1.4476W		

Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Power Plane
Layer 4		Solder Side, Microstrip signal Layer

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